

(1390 REV. 5-93) US DEPT. OF COMMERCE PATENT &amp; TRADEMARK OFFICE

ATTORNEY'S DOCKET NUMBER  
109279

**TRANSMITTAL LETTER TO THE  
UNITED STATES  
DESIGNATED/ELECTED OFFICE  
(DO/EO/US) CONCERNING A FILING  
UNDER 35 U.S.C. 371**

U.S. APPLICATION NO.  
(if known, sec 37 C.F.R.1.5)

09/807601

INTERNATIONAL APPLICATION NO.  
PCT/JP00/05395INTERNATIONAL FILING DATE  
August 11, 2000PRIORITY DATE CLAIMED  
August 19, 1999

TITLE OF INVENTION  
INTERCONNECT SUBSTRATE AND METHOD OF MANUFACTURE THEREOF, ELECTRONIC COMPONENT AND METHOD OF  
MANUFACTURING THEREOF, CIRCUIT BOARD AND ELECTRONIC INSTRUMENT

APPLICANT FOR DO/EO/US  
Nobuaki HASHIMOTO

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
  2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
  3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
  4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
  5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
    - a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
    - b. ☒ has been transmitted by the International Bureau.
    - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
  6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
  7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
    - a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
    - b. ☐ have been transmitted by the International Bureau.
    - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
    - d. ☐ have not been made and will not be made.
  8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
  9. ☒ An oath or declaration of the inventor (35 U.S.C. 371(c)(4)).
  10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
- Items 11. to 16. below concern other document(s) or information included:**
11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
  12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
  13. ☒ A FIRST preliminary amendment.  
☐ A SECOND or SUBSEQUENT preliminary amendment.
  14. ☐ A substitute specification.
  15. ☐ Entitlement to small entity status is hereby asserted.
  16. ☐ Other items or information:

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.5) <b>09/807601</b>	INTERNATIONAL APPLICATION NO. PCT/JP00/05395	ATTORNEY'S DOCKET NUMBER 109279
---	---	------------------------------------

17. <input checked="" type="checkbox"/> The following fees are submitted:  <b>Basic National fee (37 CFR 1.492(a)(1)-(5)):</b>  Search Report has been prepared by the EPO or JPO ....\$860.00  International preliminary examination fee paid to USPTO (37 CFR 1.482) .....\$690.00  No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) .....\$710.00  Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO .....\$1,000.00  International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) .....\$ 100.00  <b>ENTER APPROPRIATE BASIC FEE AMOUNT =</b>	CALCULATIONS	PTO USE ONLY																																																														
Surcharge of \$130.00 for furnishing the oath or declaration later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	\$																																																															
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 20%;">Claims</th> <th style="width: 20%;">Number Filed</th> <th style="width: 10%;">Number Extra</th> <th style="width: 10%;">Rate</th> <th style="width: 20%;"></th> <th style="width: 20%;"></th> </tr> <tr> <td>Total Claims</td> <td>39- 20 =</td> <td>19</td> <td>X \$ 18.00</td> <td>\$342.00</td> <td></td> </tr> <tr> <td>Independent Claims</td> <td>4- 3 =</td> <td>1</td> <td>X \$ 80.00</td> <td>\$80.00</td> <td></td> </tr> <tr> <td colspan="3">Multiple dependent claim(s)(if applicable)</td> <td>+ \$270.00</td> <td>\$</td> <td></td> </tr> <tr> <td colspan="4"><b>TOTAL OF ABOVE CALCULATIONS =</b></td> <td>\$1,282.00</td> <td></td> </tr> <tr> <td colspan="4">Reduction by 1/2 for filing by small entity, if applicable.</td> <td style="text-align: center;">-</td> <td>\$</td> </tr> <tr> <td colspan="4"><b>SUBTOTAL =</b></td> <td>\$1,282.00</td> <td></td> </tr> <tr> <td colspan="4">Processing fee of \$130.00 for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 month from the earliest claimed priority date (37 CFR 1.492(f)).</td> <td style="text-align: center;">+</td> <td>\$</td> </tr> <tr> <td colspan="4"><b>TOTAL NATIONAL FEE =</b></td> <td>\$1,282.00</td> <td></td> </tr> <tr> <td colspan="4" rowspan="2"></td> <td style="text-align: right;">Amount to be refunded</td> <td style="text-align: center;">\$</td> </tr> <tr> <td style="text-align: right;">Charged</td> <td style="text-align: center;">\$</td> </tr> </table>	Claims	Number Filed	Number Extra	Rate			Total Claims	39- 20 =	19	X \$ 18.00	\$342.00		Independent Claims	4- 3 =	1	X \$ 80.00	\$80.00		Multiple dependent claim(s)(if applicable)			+ \$270.00	\$		<b>TOTAL OF ABOVE CALCULATIONS =</b>				\$1,282.00		Reduction by 1/2 for filing by small entity, if applicable.				-	\$	<b>SUBTOTAL =</b>				\$1,282.00		Processing fee of \$130.00 for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 month from the earliest claimed priority date (37 CFR 1.492(f)).				+	\$	<b>TOTAL NATIONAL FEE =</b>				\$1,282.00						Amount to be refunded	\$	Charged	\$		
Claims	Number Filed	Number Extra	Rate																																																													
Total Claims	39- 20 =	19	X \$ 18.00	\$342.00																																																												
Independent Claims	4- 3 =	1	X \$ 80.00	\$80.00																																																												
Multiple dependent claim(s)(if applicable)			+ \$270.00	\$																																																												
<b>TOTAL OF ABOVE CALCULATIONS =</b>				\$1,282.00																																																												
Reduction by 1/2 for filing by small entity, if applicable.				-	\$																																																											
<b>SUBTOTAL =</b>				\$1,282.00																																																												
Processing fee of \$130.00 for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 month from the earliest claimed priority date (37 CFR 1.492(f)).				+	\$																																																											
<b>TOTAL NATIONAL FEE =</b>				\$1,282.00																																																												
				Amount to be refunded	\$																																																											
				Charged	\$																																																											

a. <input checked="" type="checkbox"/> Check No. <u>118175</u> in the amount of <u>\$1,282.00</u> to cover the above fees is enclosed. b. <input type="checkbox"/> Please charge my Deposit Account No. _____ in the amount of \$ _____ to cover the above fees. A duplicate copy of this sheet is enclosed. c. <input checked="" type="checkbox"/> The Director is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. <u>15-0461</u> . A duplicate copy of this sheet is enclosed.	<p style="text-align: center;"><b>NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.</b></p> <p>SEND ALL CORRESPONDENCE TO:          OLIFF &amp; BERRIDGE, PLC          P.O. Box 19928          Alexandria, Virginia 22320</p>
---	---

NAME: James A. Oliff  
 REGISTRATION NUMBER: 27,075  
  
 NAME: Joel S. Armstrong  
 REGISTRATION NUMBER: 36,430

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Nobuaki HASHIMOTO

Application No.: U.S. National Stage  
of PCT/JP00/05395

Filed: April 16, 2001

Docket No.: 109279

For: INTERCONNECT SUBSTRATE AND METHOD OF MANUFACTURE THEREOF,  
ELECTRONIC COMPONENT AND METHOD OF MANUFACTURE THEREOF,  
CIRCUIT BOARD AND ELECTRONIC INSTRUMENT

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office  
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE CLAIMS:

Please replace claims 12, 19, 21, 22, 31 and 38 as follows:

12. (Amended) The interconnect substrate as defined in claim 1, wherein the first and second substrates are adhered by an anisotropic conductive film including conductive particles.

19. (Amended) The electronic component as defined in claim 15, wherein: an anisotropic conductive film including conductive particles is provided on the surface of the second substrate on which the second interconnect pattern is formed; and the anisotropic conductive film adheres the first substrate to the second substrate, while also electrically connecting the second interconnect pattern to the electronic chip.

21. (Amended) A circuit board on which is mounted the electronic component as defined in claim 14.

22. (Amended) An electronic instrument equipped with the electronic component as defined in claim 14.

31. (Amended) The method of manufacture of an interconnect substrate as defined in claim 23, wherein: positioning holes are formed in the first and second substrates; and before the disposition step, a step is included in which a jig is put into the positioning holes and the first and second substrates are positioned.

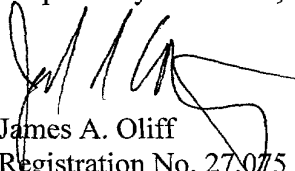
38. (Amended) The method of manufacture of an electronic component as defined in claim 32, wherein the disposition step is carried out after the first mounting step.

REMARKS

Claims 1-39 are pending. By this Preliminary Amendment, claims 12, 19, 21, 22, 31 and 38 are amended to eliminate multiple dependencies. Prompt and favorable examination on the merits is respectfully solicited.

The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. 1.121(c)(ii)).

Respectfully submitted,



James A. Oliff  
Registration No. 27,075

Joel S. Armstrong  
Registration No. 36,430

JAO:JSA/cmm

Attachment:  
Appendix

Date: April 16, 2001

**OLIFF & BERRIDGE, PLC**  
**P.O. Box 19928**  
**Alexandria, Virginia 22320**  
**Telephone: (703) 836-6400**

DEPOSIT ACCOUNT USE AUTHORIZATION Please grant any extension necessary for entry; Charge any fee due to our Deposit Account No. 15-0461
--

## APPENDIX

## Changes to Claims:

The following are marked-up versions of the amended claims:

12. (Amended) The interconnect substrate as defined in ~~any of claims 1 to 11,~~  
claim 1, wherein the first and second substrates are adhered by an anisotropic conductive film  
including conductive particles.

19. (Amended) The electronic component as defined in ~~any of claims 15 to 18,~~  
claim 15, wherein: an anisotropic conductive film including conductive particles is provided  
on the surface of the second substrate on which the second interconnect pattern is formed; and  
the anisotropic conductive film adheres the first substrate to the second substrate, while also  
electrically connecting the second interconnect pattern to the electronic chip.

21. (Amended) A circuit board on which is mounted the electronic component as  
defined in ~~any of claims 14 to 18,~~ claim 14.

22. (Amended) An electronic instrument equipped with the electronic component  
as defined in ~~any of claims 14 to 18,~~ claim 14.

31. (Amended) The method of manufacture of an interconnect substrate as  
defined in ~~any of claims 23 to 30,~~ claim 23, wherein: positioning holes are formed in the first  
and second substrates; and before the disposition step, a step is included in which a jig is put  
into the positioning holes and the first and second substrates are positioned.

38. (Amended) The method of manufacture of an electronic component as defined  
in ~~any of claims 32 to 37,~~ claim 32, wherein the disposition step is carried out after the first  
mounting step.

C/PRTS

09/807601

JG03 Rec'd OCT/90

16 APR 2001

INTERCONNECT SUBSTRATE AND METHOD OF MANUFACTURE THEREOF,  
ELECTRONIC COMPONENT AND METHOD OF MANUFACTURE THEREOF,  
CIRCUIT BOARD AND ELECTRONIC INSTRUMENT

5 TECHNICAL FIELD

The present invention relates to an interconnect substrate and method of manufacture thereof, to an electronic component and method of manufacture thereof, to a circuit board and to an electronic instrument.

10

BACKGROUND ART

In recent years the mounting density of electronic components has continued to rise, and very fine interconnect substrates are required. There is a limit to the degree to which the pattern of an interconnect substrate can be made finer when forming the interconnect pattern on one surface of the substrate only, and therefore built-up interconnect substrates have sometimes been used.

However, a built-up interconnect substrate requires repeated steps of applying an interconnect and an insulating layer, and photosensitive resin and other expensive materials, and it has therefore not been possible to reduce the cost to that of a conventional printed interconnect substrate.

25

DISCLOSURE OF THE INVENTION

The present invention solves this problem, and has as

its object the provision of an inexpensive interconnect substrate and method of manufacture thereof, an electronic component and method of manufacture thereof, a circuit board, and an electronic instrument.

5           (1) In an interconnect substrate of the present invention, a first substrate on which a first interconnect pattern is formed and a second substrate on which a second interconnect pattern is formed are disposed in superimposition;

10           at least one of the first interconnect pattern and the second interconnect pattern has a mounting region for an electronic chip; and

            the first interconnect pattern and the second interconnect pattern are electrically connected.

15           According to the present invention, the first and second substrates which are single-sided substrates are used, but the functionality of a double-sided substrate can be obtained. It should be noted that the interconnect substrate of the present invention differs from a  
20           conventional multi-layer substrate in that both of the first and second substrates have mounting regions for an electronic chip.

            (2) In this interconnect substrate,

            the second substrate may be larger than the first  
25           substrate, and the whole of the first substrate may be adhered to the second substrate.

            By means of this, the outline of the second substrate



can be an outline of the interconnect substrate, and the construction is one in which the first and second substrates are partially overlapped.

(3) In this interconnect substrate,

5       the first interconnect pattern may be formed on one surface of the first substrate;

      the second interconnect pattern may be formed on one surface of the second substrate; and

10       a surface of the first substrate opposite to the surface on which the first interconnect pattern is formed and the surface of the second substrate on which the second interconnect pattern is formed may be disposed to oppose each other.

      By means of this, the first and second interconnect  
15       patterns formed on the first and second substrates are disposed with the same alignment.

(4) In this interconnect substrate,

      a plurality of through-holes may be formed in the first substrate, and the first interconnect pattern and the  
20       second interconnect pattern may be electrically connected via the through-holes.

(5) In this interconnect substrate,

      the first interconnect pattern may pass over the through-holes;

25       the through-holes may be positioned over the second interconnect pattern; and

      a conductive material contacting the first and second

interconnect pattern may be provided within the through-holes.

(6) In this interconnect substrate,

the through-holes may be positioned over the second  
5 interconnect pattern; and

a part of the first interconnect pattern may enter the through-holes, and may be connected to the second interconnect pattern.

(7) In this interconnect substrate,

10 a plurality of through-holes may be formed in the second substrate, for the formation of a plurality of external terminals electrically connected to the second interconnect pattern and projecting from a surface of the second substrate opposite to the surface on which the  
15 second interconnect pattern is formed.

(8) In this interconnect substrate,

the through-holes formed in the first substrate and the through-holes formed in the second substrate may be formed in communicating positions.

20 (9) In this interconnect substrate,

a part of the second interconnect pattern may enter the through-holes formed in the first substrate, and may be connected to the first interconnect pattern.

(10) In this interconnect substrate,

25 a part of the first interconnect pattern and a part of the second interconnect pattern may project from a surface of the second substrate via the through-holes

formed in the second substrate and form external terminals.

(11) In this interconnect substrate,

a part of the second interconnect pattern may project into the through-holes formed in the second substrate, 5 avoiding contact with the first interconnect pattern.

(12) In this interconnect substrate,

the first and second substrates may be adhered by an anisotropic conductive film including conductive particles.

(13) In this interconnect substrate,

10 the first and second interconnect patterns may be electrically connected by the conductive particles.

(14) An electronic component of the present invention comprises:

a first substrate on which a first interconnect 15 pattern is formed;

a second substrate having a region which at least a part of the first substrate is disposed opposing, on which a second interconnect pattern is formed electrically connected to the first interconnect pattern; and

20 an electronic chip electrically connected to at least one of the first interconnect pattern and the second interconnect pattern.

According to the present invention, an interconnect substrate is used which yields the functionality of a 25 double-sided substrate by means of the first and second substrates which are single-sided substrates. It should be noted that the electronic component of the present

invention differs from an electronic component using a conventional multi-layer substrate in that both of the first and second substrates have an electronic chip mounted.

5           (15) In this electronic component,

          a surface of the first substrate opposite to a surface on which the first interconnect pattern is formed, and a surface of the second substrate on which the second interconnect pattern is formed may be adhered together.

10           By means of this, the first and second interconnect patterns formed on the first and second substrates are disposed with the same alignment.

          (16) In this electronic component,

15           a plurality of through-holes may be formed in the first substrate, and the first interconnect pattern and the second interconnect pattern may be electrically connected via the through-holes.

          (17) In this electronic component,

20           a plurality of through-holes may be formed in the second substrate; and

          external terminals electrically connected to the second interconnect pattern via the through-holes formed in the second substrate may be provided.

          (18) In this electronic component,

25           the through-holes formed in the first substrate and the through-holes formed in the second substrate may be formed in communicating positions; and

the external terminals may contact the second interconnect pattern via the through-holes formed in the second substrate, and may be provided on the first interconnect pattern via the through-holes formed in the first substrate.

(19) In this electronic component, an anisotropic conductive film including conductive particles may be provided on the surface of the second substrate on which the second interconnect pattern is formed; and

the anisotropic conductive film may adhere the first substrate to the second substrate, while also electrically connecting the second interconnect pattern to the electronic chip.

(20) In this electronic component, the second substrate may be bent to adhere a first electronic chip mounted on the first substrate to a second electronic chip mounted on the second substrate.

(21) On a circuit board of the present invention, the above-described electronic component is mounted.

(22) An electronic instrument of the present invention is equipped with the above-described electronic component.

(23) A method of manufacture of an interconnect substrate of the present invention comprises:

a disposition step of disposing at least a part of a first substrate on which a first interconnect pattern is

formed to oppose a region of a second substrate on which a second interconnect pattern is formed excluding a mounting region of an electronic chip; and

a connection step of electrically connecting the  
5 first and second interconnect patterns.

According to the present invention, using first and second substrates which are single-sided substrates, an interconnect substrate which yields the functionality of a double-sided substrate can be fabricated. It should be  
10 noted that the interconnect substrate manufactured by the method of the present invention differs from a conventional multi-layer substrate in that both of the first and second substrates have mounting regions for an electronic chip.

(24) In this method of manufacture of an interconnect  
15 substrate,

a surface of the first substrate opposite to a surface on which the first interconnect pattern is formed may be adhered to a surface of the second substrate on which the second interconnect pattern is formed, in the  
20 disposition step; and

a plurality of through-holes may be formed in the first substrate, and the first interconnect pattern may be formed to pass over the through-holes.

(25) In this method of manufacture of an interconnect  
25 substrate,

a conductive material may be provided on the first interconnect pattern via the through-holes formed in the

first substrate, before the disposition step; and

when adhering the first substrate to the second substrate in the disposition step, the conductive material may be contacted with the second interconnect pattern, 5 whereby the connection step is carried out.

By means of this, a part of the connection step is carried out in the disposition step, and thus the process can be simplified.

(26) In this method of manufacture of an interconnect 10 substrate,

a part of the first interconnect pattern may be bent into the through-holes formed in the first substrate, and connected to the second interconnect pattern, in the connection step.

(27) In this method of manufacture of an interconnect 15 substrate,

a plurality of through-holes may be formed in the second substrate; and

the through-holes formed in the first and second 20 substrates may be formed in communicating positions.

(28) In this method of manufacture of an interconnect substrate,

a part of the second interconnect pattern may be bent into the through-holes formed in the first substrate, and 25 connected to the first interconnect pattern, in the connection step.

(29) In this method of manufacture of an interconnect

substrate,

a part of the first interconnect pattern and a part of the second interconnect pattern may be integrally caused to project from a surface of the second substrate via the through-holes formed in the second substrate, to form external terminals, in the connection step.

(30) In this method of manufacture of an interconnect substrate,

a material for external terminals may be contacted with the second interconnect pattern, and provided on the first interconnect pattern via the through-holes formed in the first and second substrates, in the connection step.

By means of this, when forming the external terminals, the electrical connection of the first and second interconnect patterns can also be carried out.

(31) In this method of manufacture of an interconnect substrate,

positioning holes may be formed in the first and second substrates; and

before the disposition step, a step may be included in which a jig is put into the positioning holes and the first and second substrates are positioned.

(32) A method of manufacture of an electronic component of the present invention comprises:

a disposition step of adhering at least a part of a first substrate on which a first interconnect pattern is formed, having a mounting region for an electronic chip, to



a region of a second substrate on which a second interconnect pattern is formed excluding a mounting region for an electronic chip;

a connection step of electrically connecting the  
5 first and second interconnect patterns;

a first mounting step of mounting a first electronic chip to be electrically connected to the first interconnect pattern on the first substrate; and

a second mounting step of mounting a second  
10 electronic chip to be electrically connected to the second interconnect pattern on the mounting region of an electronic chip of the second substrate.

According to the present invention, an electronic component can be manufactured by using an interconnect  
15 substrate which yields the functionality of a double-sided substrate by means of the first and second substrates which are single-sided substrates. It should be noted that the electronic component fabricated according to the present invention differs from an electronic component using a  
20 conventional multi-layer substrate in that both of the first and second substrates have an electronic chip mounted.

(33) In this method of manufacture of an electronic component,

25 a surface of the first substrate opposite to a surface on which the first interconnect pattern is formed may be adhered to a surface of the second substrate on

which the second interconnect pattern is formed, in the disposition step; and

a plurality of through-holes may be formed in the first substrate, and the first interconnect pattern may be  
5 formed to pass over the through-holes.

(34) In this method of manufacture of an electronic component,

a plurality of through-holes may be formed in the second substrate; and

10 the through-holes formed in the first and second substrates may be formed in communicating positions.

(35) In this method of manufacture of an electronic component,

a material for external terminals may be contacted  
15 with the second interconnect pattern, and provided on the first interconnect pattern via the through-holes formed in the first and second substrates, in the connection step.

By means of this, when forming the external terminals, the electrical connection of the first and  
20 second interconnect patterns can be carried out.

(36) In this method of manufacture of an electronic component,

in the disposition step and the second mounting step, an anisotropic conductive film including conductive  
25 particles may be provided on a surface of the second substrate on which the second interconnect pattern is formed, and the first substrate may be adhered to the

second substrate by means of the anisotropic conductive film, while electrically connecting the second interconnect pattern to the second electronic chip.

By means of this, with a single material, the first  
5 substrate can be adhered to the second substrate, and the second interconnect pattern can be electrically connected to the second electronic chip, and further, these two steps can be carried out simultaneously.

(37) The electronic component may further comprise:  
10 a step in which the second substrate is bent to adhere the first electronic chip mounted on the first substrate to the second electronic chip mounted on the second substrate.

(38) In this method of manufacture of an electronic  
15 component,  
the disposition step may be carried out after the first mounting step.

(39) In this method of manufacture of an electronic  
20 component,  
the second substrate may be a part of a flexible substrate; and

the second substrate may be formed by stamping out the flexible substrate after the disposition step.

## 25 BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows the method of manufacture of an interconnect substrate according to a first embodiment of

the present invention.

Fig. 2 shows the interconnect substrate according to the first embodiment of the present invention.

Fig. 3 shows a semiconductor device according to a  
5 second embodiment of the present invention.

Fig. 4 shows a semiconductor device according to a third embodiment of the present invention.

Fig. 5 shows the method of manufacture of an interconnect substrate according to a fourth embodiment of  
10 the present invention.

Fig. 6 shows a modification of the method of manufacture of an interconnect substrate according to the fourth embodiment of the present invention.

Fig. 7 shows the method of manufacture of an interconnect substrate according to a fifth embodiment of  
15 the present invention.

Fig. 8 shows the interconnect substrate according to a sixth embodiment of the present invention.

Fig. 9 shows the method of manufacture of an interconnect substrate according to a seventh embodiment of  
20 the present invention.

Fig. 10 shows the interconnect substrate according to an eighth embodiment of the present invention.

Fig. 11 shows an electronic instrument equipped with  
25 a semiconductor device manufactured by application of the method of the present invention.

## BEST MODE FOR CARRYING OUT THE INVENTION

The present invention is now described in terms of a number of preferred embodiments, with reference to the drawings.

5

### First Embodiment

Fig. 1 illustrates the method of manufacture of the first embodiment of the interconnect substrate to which the present invention is applied, and Fig. 2 shows the first  
10 embodiment of the interconnect substrate to which the present invention is applied.

The interconnect substrate shown in Fig. 1 comprises a first substrate 10 and a second substrate 20, and can be used for example as an interposer of a semiconductor  
15 device.

The first and second substrates 10 and 20 may be formed of different materials, or may equally be formed of the same material. As the material may be used an organic material, or equally an inorganic material, or a composite  
20 of the two. As a first or second substrate 10 or 20 formed of an organic material may be used for example a flexible substrate formed of polyimide resin. As the flexible substrate may be used a tape used in FPC (Flexible Printed Circuit) or TAB (Tape Automated Bonding) technology. As the  
25 first or second substrate 10 or 20 formed of an inorganic material may be cited for example a ceramic substrate or glass substrate. As an example of a composite formation of

organic and inorganic materials may be cited for example a glass epoxy substrate. The first and second substrates 10 and 20 may be of different thicknesses or may equally be of the same thickness.

5           The size and form in plan view of the first and second substrates 10 and 20 is not particularly restricted, but in the example shown in Figs. 1 and 2, the second substrate 20 is larger than the first substrate 10.

10           On one surface of the first substrate 10 is formed an interconnect pattern 12. The interconnect pattern 12 can be formed of a conductive material such as copper or the like. The first substrate 10 has a mounting region 14 for an electronic chip such as a semiconductor chip 40 (see Fig. 3). The interconnect pattern 12 may have a pattern in the  
15 mounting region 14 corresponding to the electrodes of the electronic chip, and may have lands formed for connection to the electrodes. The interconnect pattern 12 may be adhered to the substrate 10 with an adhesive (not shown in the drawings) interposed, to form a three-layer substrate.  
20 Alternatively, the interconnect pattern 12 may be formed on the first substrate 10 without an adhesive, to form a two-layer substrate.

          On one surface of the second substrate 20 is formed an interconnect pattern 22. The interconnect pattern 22 can  
25 be formed of a conductive material such as copper or the like. The second substrate 20 has a mounting region 24 for an electronic chip such as a semiconductor chip 42 (see

Fig. 3), and a region 26 to which at least a part of the first substrate 10 is adhered. The interconnect pattern 22 is formed to span both the mounting region 24 and the region 26. The second interconnect pattern 22 is  
5 electrically connected to the first interconnect pattern 12.

In the mounting region 24, the interconnect pattern 22 may have a pattern corresponding to the electrodes of the electronic chip, and may have lands formed for  
10 connection to the electrodes. The interconnect pattern 22 may be adhered to the substrate 20 with an adhesive (not shown in the drawings) interposed, to form a three-layer substrate. Alternatively, the interconnect pattern 22 may be formed on the second substrate 20 without an adhesive,  
15 to form a two-layer substrate.

In the region 26 of the second substrate 20, at least a part of the first substrate 10 is adhered. For this adhesion, for example an adhesive 16 can be used. If the first substrate 10 is smaller in plane extent than the  
20 second substrate 20, the whole of the first substrate 10 may be adhered to the region 26 of the second substrate.

The surface of the first substrate 10 opposite to that on which the first interconnect pattern 12 is formed may be adhered to the surface of the second substrate 20 on  
25 which the second interconnect pattern 22 is formed. In this case, between the first and second interconnect patterns 12 and 22, since the first substrate 10 is interposed, for the

purposes of electrical connection between the two, a plurality of through-holes 18 are formed in the first substrate 10. In the through-holes 18, a conductive material 19 of solder or the like is provided, and by means of the conductive material 19, electrical conduction between the first and second interconnect patterns 12 and 22 is achieved. More specifically, if the first interconnect pattern 12 passes over the through-holes 18, and the through-holes 18 are positioned over the second interconnect pattern 22, then by means of the conductive material 19 provided within the through-holes 18, the electrical connection of the first and second interconnect patterns 12 and 22 can be achieved. The first and second interconnect patterns 12 and 22 are preferably plated with solder, tin, gold, nickel, or the like.

In the second substrate 20, through-holes 28 are formed. The through-holes 28 serve for electrical connection of a plurality of external terminals 44 (see Fig. 3) to the second interconnect pattern 22. That is to say, the external terminals 44 projecting to the surface of the second substrate 20 opposite to that on which the second interconnect pattern 22 is formed can be electrically connected to the second interconnect pattern 22 via the through-holes 28. For example, if the second interconnect pattern 22 passes over the through-holes 28, then the external terminals 44 can be provided on the second interconnect pattern 22 via the through-holes 28.



The through-holes 18 formed in the first substrate 10, and the through-holes 28 formed in the second substrate 20 may be formed in communicating positions. However, through-holes 18 and 28 do not actually need to  
5 communicate, and may be blocked by the second interconnect pattern 22 or the like.

In this embodiment of the interconnect substrate, an inexpensive single-sided substrate is used, and has the functions of a built-up substrate or multi-layer substrate.  
10 That is to say, the first interconnect pattern 12 of the first substrate 10 and the second interconnect pattern 22 of the second substrate 20 are superimposed, and therefore a finely detailed interconnect is possible. Since both first and second substrates 10 and 20 have the mounting  
15 regions 14 and 24, a plurality of electronic chips such as the semiconductor chips 40 and 42 (see Fig. 3) or the like can be mounted.

This embodiment of the interconnect substrate is constructed as described above, and the method of  
20 manufacture thereof is now described.

First, the first and second substrates 10 and 20 are taken. The first and second substrates 10 and 20 can be formed by stamping out a flexible substrate. The flexible substrate may be in a tape form. The flexible substrate may  
25 first have the first or second interconnect patterns 12 and 22 or through-holes 18 and 28, and so on formed, before the stamping out.

When the second substrate 20 is formed by stamping out a flexible substrate, the first substrate 10 may be adhered to the flexible substrate before the stamping out. Furthermore, a first flexible substrate on which a plurality of first substrates 10 are formed may be adhered to a second flexible substrate on which a plurality of second substrates 20 are formed, and the second flexible substrate stamped out to the external form of each of the second substrates 20. By doing this, the first substrates 10 are also cut apart.

Then a disposition step, adhering at least a part of the first substrate 10 to the region 26 of the second substrate 20 excluding the electronic component mounting region 24, and a step of connection, electrically connecting the first and second interconnect patterns 12 and 22, are carried out.

Before the disposition step, or as part of the disposition step, positioning of the first and second substrates 10 and 20 is preferably carried out. For example, as shown in Fig. 1, positioning holes 30 and 32 may be formed in the first and second substrates 10 and 20 so as to be communicating when the positioning is achieved, and the positioning carried out by inserting a jig 34 consisting of pins or the like.

In the disposition step, the surface of the first substrate 10 opposite to that on which the first interconnect pattern 12 is formed, and the surface of the

second substrate 20 on which the second interconnect pattern 22 is formed, may be adhered. For the adhesion, the adhesive 16 may be used.

The adhesive 16 may be provided in sheet form, may be  
5 provided as a liquid or gel. When provided in sheet form, the adhesive 16 exhibits adhesion as a result of the application of heat and pressure. The characteristics of the adhesive 16 may be either thermosetting or thermoplastic. As the adhesive 16 may be used a sheet form  
10 of epoxy resin, or a thermoplastic polyimide resin may be used.

The adhesive 16 may be provided on at least either of the first substrate 10 and second substrate 20. When the adhesive 16 used is insulating, the adhesive 16 is  
15 preferably provided avoiding the electrical connection portion of the first and second interconnect patterns 12 and 22. In more detail, the adhesive 16 is provided to avoid the conductive material 19 and the bonding portion of the second interconnect pattern 22 with the conductive  
20 material 19. For example, when the adhesive 16 is adhered in sheet form to the first substrate 10, the portions of the adhesive 16 overlying the position of formation of the conductive material 19 may first have holes formed, after which the adhesive 16 is adhered to the first substrate 10.  
25 Such holes may be formed by stamping using a jig not shown in the drawings.

Alternatively, after adhering the adhesive 16 to the

first substrate 10, at the same time as forming the through-holes 18 in the first substrate 10, holes may be formed in the adhesive 16 to communicate with the through-holes 18. By means of this, a separate step of forming  
5 holes in the adhesive 16 can be omitted. In this case, since when the first substrate 10 is formed the adhesive 16 is already adhered, the adhesive 16 is selected not to lose its adhesive force as a result of heat applied in process steps until the first and second substrates 10 and 20 are  
10 adhered. For example, the adhesive 16 may employ a thermoplastic substance (for example thermoplastic polyimide resin).

By means of the disposition step, a part of the step of connection may be carried out. For example, before the  
15 disposition step the conductive material 19 is provided in the through-holes 18 formed in the first substrate 10. As the conductive material 19 can be used solder, high-temperature solder, cream solder, or the like. Then in the disposition step, when the first and second substrates 10  
20 and 20 are adhered, the conductive material 19 contacts the second interconnect pattern 22, whereby at least a part of the connection step may be carried out.

If the conductive material 19 is soft, the conductive material 19 is provided in the through-holes 18 to the  
25 extent of overflowing from the surface of the first substrate 10 or when the adhesive 16 is provided the surface thereof. By doing this, by means of the disposition

step, the first and second interconnect patterns 12 and 22 can be electrically connected.

If the conductive material 19 is hard at room temperature, then after the disposition step, the  
5 conductive material 19 is heated and fused, so that the first and second interconnect patterns 12 and 22 are electrically connected. The heating may be carried out in a reflow process when forming the external terminals 44 (see Fig. 3), or when mounting the semiconductor device on a  
10 circuit board.

In the above embodiment, an example was described in which substrates with an interconnect pattern formed on one side of the substrate are superimposed together, but within the range in which superimposing two substrates is less  
15 costly, multi-layer substrates including built-up substrates may be superimposed together, or a multi-layer substrate and a single-sided substrate may be superimposed together.

In the above embodiment, the construction was  
20 described in which through the upper substrate the interconnect patterns of the upper and lower substrates are connected together, but the construction is also possible in which the interconnect pattern of the upper substrate and the interconnect pattern of the lower substrate oppose  
25 each other to be connected.

Furthermore, in the above embodiment, an example is shown in which the second substrate 20 extends in one

direction only from the first substrate 10, but this may equally extend in a plurality of directions (two directions, three directions, or four directions).

Furthermore, at least a part of the interconnect patterns 12 and 22 of the first and second substrates 10 and 20 may be formed as a jumper lead spanning the interconnect pattern of the other substrate. By doing this, even if a multi-layer interconnect pattern is required on the substrate, using the single-sided substrates, a multi-layer construction can effectively be obtained at low cost.

A semiconductor device can also be constructed using an interconnect substrate fabricated in this way. The content described in this embodiment can, insofar as is possible also be applied to the following embodiments.

#### Second Embodiment

Fig. 3 shows a second embodiment of the semiconductor device to which the present invention is applied. This embodiment of the semiconductor device includes the interconnect substrate explained in the first embodiment. The interconnect substrate is as explained in the first embodiment, detailed description is omitted. The surface of the first substrate 10 opposite to that on which the first interconnect pattern 12 is formed is adhered to the surface of the second substrate 20 on which the second interconnect pattern 22 is formed.

In the mounting region 14 of the first substrate 10,

the semiconductor chip 40 is mounted. The semiconductor chip 40 is electrically connected to the first interconnect pattern 12. In more detail, electrodes 41 of the semiconductor chip 40 are electrically connected to the first interconnect pattern 12. The electrodes 41 are commonly bonded to lands of the interconnect pattern 12. On at least either of the part of the interconnect pattern 12 connecting to the electrodes 41, and the electrodes 41, bumps may be formed. For the bond between the interconnect pattern 12 and the electrodes 41, an anisotropic conductive film, solder, or a conductive paste, or the like may be used, or metal bonding using ultrasound may be applied. To the ultrasound may be added the application of heat or pressure. As shown in Fig. 3, the semiconductor chip 40 may be mounted so that the electrodes 41 are positioned over the through-holes 18, or may be mounted to avoid the through-holes 18. In the latter case, the distance from the external terminals 44 is increased, and the transmission of force is reduced, thus allowing improved reliability. The same is true also of the following embodiments.

In the mounting region 24 of the second substrate 20, the semiconductor chip 42 is mounted. The semiconductor chip 42 is electrically connected to the second interconnect pattern 22. In more detail, electrodes 43 of the semiconductor chip 42 and the second interconnect pattern 22 are electrically connected. In this respect, the details described above relating to the connection of the

semiconductor chip 40 and the first interconnect pattern 12 may be applied. Between each of the semiconductor chips 40 and 42 and the first and second substrates 10 and 20, interposing a resin such as an underfill or the like not shown in the drawings is preferable from the viewpoint of increased reliability.

A plurality of external terminals 44 electrically connected to the second interconnect pattern 22 are provided on the second substrate 20. The external terminals 44 are provided on the surface of the second substrate 20 opposite to that on which the second interconnect pattern 22 is formed. For example, the external terminals 44 may be provided on the second interconnect pattern 22 via the through-holes 28 formed in the second substrate 20. The external terminals 44 can be formed of solder or the like. For example, cream solder may be provided in the through-holes 28 so as to project above the surface, and this may be fused to form ball-form terminals. Alternatively, solder may be provided in the through-holes 28, and plating with a conductive material applied, then solder balls mounted to form the external terminals 44.

In the description above, the mounting of the semiconductor chip on the interconnect pattern is described as being carried out by the face-down method, but equally, the face-up method by wire bonding, or the TAB method by flying leads may be applied. The above described method of mounting the semiconductor chip on the interconnect pattern



may be used in the embodiments described below.

By means of this embodiment of the semiconductor device, since it is used as the interposer for an interconnect substrate described in the first embodiment,  
5 the cost can be reduced.

This embodiment is constructed as described above, and the method of manufacture thereof is now described.

#### First example of the method of manufacture

10 In this example, the interconnect substrates already described in the first embodiment are taken, semiconductor chips 40 and 42 are mounted thereon, and external terminals 44 are provided. Since the details thereof will be clear from the above description, further description is omitted.

15

#### Second example of the method of manufacture

In this example, the first and second substrates 10 and 20 are taken. Then before the first and second substrates 10 and 20 are adhered to constitute an  
20 interconnect substrate, at least one of the semiconductor chips 40 and 42 is mounted. For example, the semiconductor chip 40 is mounted on the mounting region 14 of the first substrate 10, and the semiconductor chip 42 is mounted on the mounting region 24 of the second substrate 20, and then  
25 the first and second substrates 10 and 20 are adhered.

Alternatively, one of the semiconductor chips 40 and 42 is mounted one of the mounting regions 14 and 24 of the

first and second substrates 10 and 20, and the first and second substrates 10 and 20 are adhered, after which the other of the semiconductor chips 40 and 42 is mounted on the other of the mounting regions 14 and 24 of the first and second substrates 10 and 20.

When the first or second substrate 10 or 20 is formed by stamping out a flexible substrate, the semiconductor chip 40 or 42 may be mounted on the flexible substrate first, and then the first or second substrate 10 or 20 formed by stamping out.

When the second substrate 20 is formed by stamping out a flexible substrate, the first substrate 10 may be mounted on the flexible substrate before stamping out this flexible substrate to form the second substrate. In this case, the semiconductor chip 40 may be already mounted on the first substrate 10.

A plurality of first semiconductor chips 40 may be mounted on a first flexible substrate which is to form a plurality of first substrates 10, and this first flexible substrate adhered to a second flexible substrate which is to form a plurality of second substrates 20. Then the second flexible substrate may be stamped out to the outline form of the second substrates 20. By this means, the first flexible substrate is also cut to the outline form of the first substrate 10.

On the second substrate 20, a plurality of external terminals 44 are provided. This step may be carried out

after forming the first and second substrates 10 and 20 and adhering the two together, and mounting the first and second semiconductor chips 40 and 42 on the first and second substrates 10 and 20, but is not limited by this.

5 For example, the step of providing the external terminals 44 may be carried out before forming the second substrates 20, by provision beforehand on the second flexible substrate which is to form a plurality of second substrates 20. The step of providing the external terminals 44 may be

10 carried out before mounting the second semiconductor chip 42 on the second substrate 20.

In this example, to the mutual relationship between the first and second substrates 10 and 20, the construction of the adherence of the two, the electrical connection

15 construction, and so on, the description in the first embodiment can be applied, and the same is true of the method of manufacture.

When at least a part of the interconnect pattern of the first or second substrate 10 or 20 is formed as jumper

20 leads, a semiconductor chip may be mounted on at least one of the substrates, and a multi-layer construction may effectively be achieved. This can also be applied to all of the following embodiments.

### 25 Third Embodiment

Fig. 4 shows a third embodiment of the semiconductor device to which the present invention is applied. This

embodiment of the semiconductor device includes the structural elements of the semiconductor device described in the second embodiment, and as these structural elements are the same as described in the second embodiment, 5 detailed description is omitted here. The surface of the first substrate 10 opposite to that on which the first interconnect pattern 12 is formed is adhered to the surface of the second substrate 20 on which the second interconnect pattern 22 is formed.

10 In this embodiment, the second substrate 20 is bent. The first semiconductor chip 40 and second semiconductor chip 42 are adhered. In more detail, the surface of the first semiconductor chip 40 opposite to the surface of mounting on the first substrate 10, and the surface of the 15 second semiconductor chip 42 opposite to the surface of mounting on the second substrate 20 are adhered. For the adhesion, an adhesive 50 can be used. Alternatively, a tacky adhesive can be used, or crimping, flip, or other mechanical methods may be used to maintain the bent state 20 of the second substrate 20.

According to this embodiment of the semiconductor device, the first and second semiconductor chips 40 and 42 are overlaid to save space. When the second substrate 20 extends beyond the first substrate 10 in a plurality of 25 directions, the second substrate 20 may be bent over in a plurality of directions. When a plurality of semiconductor chips are mounted, the second substrate 20 may be folded

between the semiconductor chips.

The method of manufacture of this embodiment of the semiconductor device adds to the method of manufacture of the above described semiconductor device described in the second embodiment, a step of bending the second substrate 20, and adhering together the first semiconductor chip 40 mounted on the first substrate 10 and the second semiconductor chip 42 mounted on the second substrate 20. It should be noted that the external terminals 44 may be provided before bending the second substrate 20, or may be provided after bending the second substrate 20.

In Fig. 4, a semiconductor device fabricated in this way is mounted on a circuit board 52. For the circuit board 52 is generally used an organic substrate such as for example a glass epoxy substrate or the like. On the circuit board 52, an interconnect pattern 54 of for example copper is formed into a desired circuit, and the interconnect pattern 54 and the external terminals 44 of the semiconductor device are connected to achieve electrical conduction therebetween.

#### Fourth Embodiment

Fig. 5 shows a fourth embodiment of the interconnect substrate to which the present invention is applied. In this embodiment, a part of the first interconnect pattern 12 enters into the through-holes 18 formed in the first substrate 10, to connect to the second interconnect pattern

22. In more detail, within the through-holes 18, bent portions 60 formed from a part of the first interconnect pattern 12 are formed by pressing with a projection die 62. The bent portions 60 contact the second interconnect pattern 22. When the second interconnect pattern 22 within the through-holes 28 is bent, if supported from the direction opposite to the direction of application of pressure, the contact will be made easier. The projection die 62, either individually, or at a plurality of points, may be heated, and the bent portions 60 and second interconnect pattern 22 soldered or brazed, or may be bonded with a conductive adhesive or the like. Ultrasound bonding may be applied by applying ultrasound to the projection die 62. In place of the projection die 62, a single-point bonder may be used, and the bent portions 60 and second interconnect pattern 22 bonded one point at a time. On this occasion, the second interconnect pattern 22 within the through-holes 28 may be supported from the direction opposite to the direction of application of pressure during the bending. A precondition for this is that the through-holes 18 formed in the first substrate 10 are positioned over the second interconnect pattern 22. It should be noted that the bent portions 60 may partially rupture. To other aspects of the construction the description in the first embodiment can be applied. The surface of the first substrate 10 opposite to that on which the first interconnect pattern 12 is formed is adhered to

the surface of the second substrate 20 on which the second interconnect pattern 22 is formed.

According to this embodiment, by means of the bent portions 60 the electrical connection of the first and second interconnect patterns 12 and 22 is achieved. As shown in Fig. 5, the through-holes 18 formed in the first substrate 10 and the through-holes 28 formed in the second substrate 20 may be formed in communicating positions. In this case, when the second interconnect pattern 22 is formed over the through-holes 28, a part of the second interconnect pattern 22 may enter the through-holes 28.

Alternatively, as shown in Fig. 6, the through-holes 18 formed in the first substrate 10 and the through-holes 28 formed in the second substrate 20 may be formed in offset positions. In this case, the bent portion 64 contacts or is bonded to a part of the second interconnect pattern 22 in intimate contact with the second substrate 20. The method for this is as described above.

The method of manufacture of this embodiment of the interconnect substrate uses the projection die 62 to press a part of the first interconnect pattern 12 into the through-holes 18. In more detail, the first interconnect pattern 12 passes over the through-holes 18 of the first substrate 10, and the part of the first interconnect pattern 12 over the through-holes 18 is pressed into the through-holes 18 by the projection die 62. In this way, the bent portions 60 can be formed. In that case, the second

substrate 20 can be supported in the plane by a jig. This step is a connection step in which the first and second interconnect patterns 12 and 22 are electrically connected. It should be noted that the bent portions 60 may be formed in such a way that a part thereof is ruptured. The step of forming the bent portions 60 and the connection step allow the second interconnect pattern 22 to be bonded while bending the first interconnect pattern 12 in a single step, thus in this case reducing the number of steps.

When connecting the bent portions 60 and the second interconnect pattern 22, pressure is preferably applied to the bent portions 60 while squashing a part of the adhesive 16 out of the way, to cause an electrical connection to the second interconnect pattern. In this case, the adhesive 16 is preferably provided as a liquid or gel. In more detail, first, the adhesive 16 is provided on at least one of the first and second substrates 10 and 20 to include the portion of electrical connection between the two. Thereafter, before curing the adhesive 16, pressure is applied to the bent portions 60 in the direction of the second interconnect pattern 22, whereby a part of the adhesive 16 is squashed away to the outside of the bent portions 60. In this case, if ultrasonic vibration is applied to the bent portions 16, the electrical bond can be positively made. By means of this, it is not necessary to provide the adhesive 16 between the bent portions 60 and the second interconnect pattern 22, and the reliability of



the electrical connection between the two is increased. It should be noted that this method can, insofar as is possible, be applied to all of the embodiments.

In this way, a semiconductor device using the thus  
5 fabricated interconnect substrate as an interposer can also be constructed.

#### Fifth Embodiment

Fig. 7 shows a fifth embodiment of the interconnect  
10 substrate to which the present invention is applied. In this embodiment, a part of the second interconnect pattern 22 enters the through-holes 18 formed in the first substrate 10, to contact the first interconnect pattern 12. In more detail, within the through-holes 18, bent portions  
15 66 are formed from a part of the second interconnect pattern 22. The bent portions 66 contact or are bonded to the first interconnect pattern 12. It should be noted that the bent portions 66 may, as shown in Fig. 7, partially rupture, or may be of a continuous form without rupture, as  
20 in the bent portions 60 shown in Fig. 5. To other respects of the constitution, and the method of forming and of bonding the description in the above described embodiments can be applied. It should be noted that the surface of the first substrate 10 opposite to that on which the first  
25 interconnect pattern 12 is formed is adhered to the surface of the second substrate 20 on which the second interconnect pattern 22 is formed. According to this embodiment, by

means of the bent portions 66, electrical connection of the first and second interconnect patterns 12 and 22 is achieved.

In the method of manufacture of this embodiment of the interconnect substrate, using a projection die 68, a part of the second interconnect pattern 22 is pressed into the through-holes 18. To carry out this step, it is preferable that the through-holes 28 of the second substrate 20 and the through-holes 18 of the first substrate 10 are formed in communicating positions.

In more detail, the projection die 68 is inserted into the through-holes 28 from the surface of the second substrate 20 opposite to that on which the second interconnect pattern 22 is formed. Then by means of the projection die 68, the second interconnect pattern 22 is pressed into the through-holes 18, and bonded to the first interconnect pattern 12. In this way, the bent portions 66 can be formed. This step is a connection step of electrically connecting the first and second interconnect patterns 12 and 22. Naturally, a plurality of points (plurality of locations) may be bonded in a single operation with a projection die having a plurality of projections.

In this way, a semiconductor device using the thus fabricated interconnect substrate as an interposer can also be constructed.

### Sixth Embodiment

Fig. 8 shows a sixth embodiment of the interconnect substrate to which the present invention is applied. In this embodiment, the surface of the first substrate 10 opposite to that on which the first interconnect pattern 12 is formed is adhered to the surface of the second substrate 20 on which the second interconnect pattern 22 is formed.

A part of the second interconnect pattern 22 enters the through-holes 28 formed in the second substrate 20 to form external terminals 70. The second interconnect pattern 22 forms at least the outer wall of the external terminals 70. A part of the first interconnect pattern 12 enters the through-holes 18 and 28 formed in the first and second substrates 10 and 20, and connects, and contacts or is bonded with the second interconnect pattern 22.

The through-holes 18 formed in the first substrate 10 and the through-holes 28 formed in the second substrate 20 are formed in communicating positions. A part of the first interconnect pattern 12 enters the through-holes 28 of the second substrate 20, to form the internal wall of the external terminals 70. In other respects, the constitution, and the method of formation of any of the above described embodiments can be applied.

According to this embodiment, the external terminals 70 are formed from a part of the second interconnect pattern 22 or a part of the first and second interconnect

patterns 12 and 22, and therefore a separate element for the external terminals is not required, and the component count can be reduced.

In the method of manufacture of this embodiment of the interconnect substrate, using the projection die 62 shown in Fig. 5, a part of the first interconnect pattern 12 is pressed into the through-holes 18, and furthermore, the second interconnect pattern 22 is pressed into the through-holes 28. When the external terminals 70 are to project beyond the second substrate 20, a part of the second interconnect pattern 22 is caused to project from the second substrate 20. When it is not necessary for the external terminals 70 to project beyond the second substrate 20, a part of the second interconnect pattern 22 may be fixed within the through-holes 28.

In the method of manufacture of this embodiment, the description of the method of manufacture in any of the above described embodiments can be applied. In this way, a semiconductor device using the thus fabricated interconnect substrate as an interposer can also be constructed.

In the fourth to sixth embodiments, if the gap between the first substrate 10 and second substrate 20 is adhered, the adhesion strength between the substrates increases, and the semiconductor device reliability is increased, which is even more preferable.

#### Seventh Embodiment

Fig. 9 is a figure showing the method of manufacture of a seventh embodiment of the interconnect substrate to which the present invention is applied. In this embodiment, in a step of disposition of the first and second substrates 10 and 20 an anisotropic conductive film 72 is used. That is to say, between the first and second substrates 10 and 20, the anisotropic conductive film 72 is interposed, to adhere the two. It should be noted that the anisotropic conductive film 72 may be an anisotropic conductive material already in tape form or sheet form, or may be a liquid anisotropic conductive material applied to at least one of the first and second substrates 10 and 20. The anisotropic conductive material has conductive particles dispersed in an adhesive. It should be noted that the surface of the first substrate 10 opposite to that on which the first interconnect pattern 12 is formed is adhered to the surface of the second substrate 20 on which the second interconnect pattern 22 is formed.

When the anisotropic conductive film 72 is provided on the surface of the second substrate 20 on which the second interconnect pattern 22 is formed, the second semiconductor chip 42 may be subjected to face-down bonding to the second substrate 20, with the anisotropic conductive film 72 interposed. In this case, the anisotropic conductive film 72 is preferably provided on both of the mounting region 24 for mounting the second semiconductor chip 42 and the region 26 of the second substrate 20 for

adhering the first substrate 10. Then the step of disposition of the first and second substrates 10 and 20, and the second mounting step for the second semiconductor chip 40 can both be carried out at the same time, or one  
5 may be carried out, followed by the other.

By means of this, the material for adhering the first and second substrates 10 and 20 and the material for adhering the second semiconductor chip 42 to the second substrate 20 while forming an electrical connection are the  
10 same material. As a result, the component count can be reduced.

In the example shown in Fig. 9, after the step of disposition of the first and second substrates 10 and 20, the second mounting step for the second semiconductor chip  
15 42, and an electrical connection step for the first and second interconnect patterns 12 and 22 are carried out. In more detail, in Fig. 9, between the first and second substrates 10 and 20 the anisotropic conductive film 72 is interposed, and the anisotropic conductive film 72 is also  
20 provided over the mounting region 24 for the second semiconductor chip 42 of the second substrate 20.

The second semiconductor chip 42 and the second substrate 20 are subjected to pressure by means of a pressure jig 74, and the second semiconductor chip 42 is  
25 subjected to face-down bonding to the second substrate 20. That is to say, the second mounting step for the second semiconductor chip 40 is carried out.

Using the projection die 62, in the same step as the step shown in Fig. 5, the first and second interconnect patterns 12 and 22 are electrically connected. That is to say, a connection step is carried out. Furthermore, using the projection die 62, by the same step as the step shown in Fig. 8, the external terminals 70 may be formed. In this embodiment, since the anisotropic conductive film 72 is interposed between the first and second interconnect patterns 12 and 22, the first and second interconnect patterns 12 and 22 may be electrically connected by the conductive particles.

It should be noted that in this embodiment, if the mounting step of the semiconductor chip 42 is eliminated, an interconnect substrate can be fabricated. The construction of this interconnect substrate is the content of the above description, with the semiconductor chip 42 eliminated.

#### Eighth Embodiment

Fig. 10 shows an eighth embodiment of the interconnect substrate to which the present invention is applied. In this embodiment, the through-holes 18 and 28 of the first and second substrates 10 and 20 are formed in communicating positions. The first interconnect pattern 12 passes over the through-holes 18. A part of the second interconnect pattern 22 preferably projects into the through-holes 28 as exemplified by the projections 82 shown

in Fig. 10, but as long as there is a space for the second interconnect pattern 22 and through-holes 28 to communicate, need not thus project. It is not required for a part of the second interconnect pattern 22 to contact the first interconnect pattern 12, but it may thus contact. It should be noted that the surface of the first substrate 10 opposite to that on which the first interconnect pattern 12 is formed is adhered to the surface of the second substrate 20 on which the second interconnect pattern 22 is formed.

10 In the communicating through-holes 18 and 28, a conductive material such as solder or the like is provided, and external terminals 80 are formed. The conductive material may be provided on the first interconnect pattern 12. The conductive material may be provided within the through-holes 28 in the second interconnect pattern 22, and bonded to the projections 82. By doing this, a single step of providing the conductive material is sufficient, and a shortening of the process can be achieved. Alternatively, the conductive material may contact the surface of at least a part of the second interconnect pattern 22. The conductive material constituting the external terminals 80 electrically connects the first and second interconnect patterns 12 and 22 via the through-holes 18 and 28.

25 According to this embodiment, by means of the conductive material electrically connecting the first and second interconnect patterns 12 and 22, the external terminals 80 can be formed integrally. Alternatively, the



conductive material electrically connecting the first and second interconnect patterns 12 and 22 may be provided in the communicating through-holes 18 and 28, and solder balls or the like provided separately as terminal material.

5           In the method of manufacture of this embodiment of the interconnect substrate, first and second substrates 10 and 20, on which the first and second interconnect patterns 12 and 22 of the above described construction are formed, are adhered, and the conductive material is provided within  
10 the communicating through-holes 18 and 28. Then this conductive material is heated and fused, or solder balls or the like are provided as terminal material on this conductive material, to form the external terminals 80.

          Using the interconnect substrate thus obtained, a  
15 semiconductor device may be fabricated. As part of the fabrication process of the semiconductor device, this embodiment may be applied.

          Furthermore, in all of the above described embodiments, a construction with a plurality of substrates  
20 overlaid may be adopted. In this case, if the directions of extension of the overlaid substrates are such that the semiconductor chip is exposed, the mounting characteristics will be improved. Further in all of the embodiments, on each single substrate a plurality of semiconductor chips  
25 may be mounted.

          In all of the above described embodiments, the external terminals 44 are not necessarily required, and a

various means of extending the interconnects to the exterior may be used, as for example extensions of a substrate can be used as connectors, or connectors may be mounted, or other passive parts may be mounted on the  
5 substrate to complete a semiconductor module.

As an electronic instrument having the semiconductor device to which the present invention is applied, Fig. 11 shows a notebook personal computer 100.

It should be noted that in the embodiments described  
10 above, "semiconductor chip" may be replaced by "electronic chip" (whether an active element or a passive element) which can be mounted on a substrate to manufacture an electronic component. Alternatively, a combination of semiconductor chips and electronic chips may be used. As  
15 electronic components manufactured using such an electronic chip may be cited, for example, optical elements, resistors, capacitors, coils, oscillators, filters, temperature sensors, thermistors, varistors, variable resistors, and fuses.

20

## CLAIMS

1. An interconnect substrate wherein:

a first substrate on which a first interconnect  
5 pattern is formed and a second substrate on which a second  
interconnect pattern is formed are disposed in  
superimposition;

at least one of the first interconnect pattern and  
the second interconnect pattern has a mounting region for  
10 an electronic chip; and

the first interconnect pattern and the second  
interconnect pattern are electrically connected.

2. The interconnect substrate as defined in claim 1,

15 wherein the second substrate is larger than the first  
substrate, and the whole of the first substrate is adhered  
to the second substrate.

3. The interconnect substrate as defined in claim 1,

20 wherein:

the first interconnect pattern is formed on one  
surface of the first substrate;

the second interconnect pattern is formed on one  
surface of the second substrate; and

25 a surface of the first substrate opposite to the  
surface on which the first interconnect pattern is formed  
and the surface of the second substrate on which the second

interconnect pattern is formed are disposed to oppose each other.

4. The interconnect substrate as defined in claim 3,

5 wherein a plurality of through-holes are formed in the first substrate, and the first interconnect pattern and the second interconnect pattern are electrically connected via the through-holes.

10 5. The interconnect substrate as defined in claim 4, wherein:

the first interconnect pattern passes over the through-holes;

15 the through-holes are positioned over the second interconnect pattern; and

a conductive material contacting the first and second interconnect pattern is provided within the through-holes.

20 6. The interconnect substrate as defined in claim 4, wherein:

the through-holes are positioned over the second interconnect pattern; and

25 a part of the first interconnect pattern enters the through-holes, and is connected to the second interconnect pattern.

7. The interconnect substrate as defined in claim 4,

wherein a plurality of through-holes are formed in the second substrate, for the formation of a plurality of external terminals electrically connected to the second interconnect pattern and projecting from a surface of the second substrate opposite to the surface on which the second interconnect pattern is formed.

8. The interconnect substrate as defined in claim 7, wherein the through-holes formed in the first substrate and the through-holes formed in the second substrate are formed in communicating positions.

9. The interconnect substrate as defined in claim 8, wherein a part of the second interconnect pattern enters the through-holes formed in the first substrate, and is connected to the first interconnect pattern.

10. The interconnect substrate as defined in claim 8, wherein a part of the first interconnect pattern and a part of the second interconnect pattern project from a surface of the second substrate via the through-holes formed in the second substrate and form external terminals.

11. The interconnect substrate as defined in claim 8, wherein a part of the second interconnect pattern projects into the through-holes formed in the second substrate, avoiding contact with the first interconnect

pattern.

12. The interconnect substrate as defined in any of claims 1 to 11,

5            wherein the first and second substrates are adhered by an anisotropic conductive film including conductive particles.

13. The interconnect substrate as defined in claim 12,

10           wherein the first and second interconnect patterns are electrically connected by the conductive particles.

14. An electronic component comprising:

15           a first substrate on which a first interconnect pattern is formed;

             a second substrate having a region which at least a part of the first substrate is disposed opposing, on which a second interconnect pattern is formed electrically connected to the first interconnect pattern; and

20           at least one electronic chip electrically connected to at least one of the first interconnect pattern and the second interconnect pattern.

15. The electronic component as defined in claim 14,

25           wherein a surface of the first substrate opposite to a surface on which the first interconnect pattern is formed, and a surface of the second substrate on which the

second interconnect pattern is formed are adhered together.

16. The electronic component as defined in claim 15,

wherein a plurality of through-holes are formed in  
5 the first substrate, and the first interconnect pattern and  
the second interconnect pattern are electrically connected  
via the through-holes.

17. The electronic component as defined in claim 16,

10 wherein:

a plurality of through-holes are formed in the second  
substrate; and

external terminals electrically connected to the  
second interconnect pattern via the through-holes formed in  
15 the second substrate are provided.

18. The electronic component as defined in claim 17,  
wherein:

the through-holes formed in the first substrate and  
20 the through-holes formed in the second substrate are formed  
in communicating positions; and

the external terminals contact the second  
interconnect pattern via the through-holes formed in the  
second substrate, and are provided on the first  
25 interconnect pattern via the through-holes formed in the  
first substrate.

19. The electronic component as defined in any of claims 15 to 18, wherein:

an anisotropic conductive film including conductive particles is provided on the surface of the second substrate on which the second interconnect pattern is formed; and

the anisotropic conductive film adheres the first substrate to the second substrate, while also electrically connecting the second interconnect pattern to the electronic chip.

20. The electronic component as defined in claim 19 which comprises first and second electronic chips,

wherein the second substrate is bent to adhere the first electronic chip mounted on the first substrate to the second electronic chip mounted on the second substrate.

21. A circuit board on which is mounted the electronic component as defined in any of claims 14 to 18.

22. An electronic instrument equipped with the electronic component as defined in any of claims 14 to 18.

23. A method of manufacture of an interconnect substrate comprising:

a disposition step of disposing at least a part of a first substrate on which a first interconnect pattern is



formed to oppose a region of a second substrate on which a second interconnect pattern is formed excluding a mounting region of an electronic chip; and

a connection step of electrically connecting the  
5 first and second interconnect patterns.

24. The method of manufacture of an interconnect substrate as defined in claim 23, wherein:

in the disposition step, a surface of the first  
10 substrate opposite to a surface on which the first interconnect pattern is formed is adhered to a surface of the second substrate on which the second interconnect pattern is formed; and

a plurality of through-holes are formed in the first  
15 substrate, and the first interconnect pattern is formed to pass over the through-holes.

25. The method of manufacture of an interconnect substrate as defined in claim 24, wherein:

20 before the disposition step, a conductive material is provided on the first interconnect pattern via the through-holes formed in the first substrate; and

when adhering the first substrate to the second substrate in the disposition step, the conductive material  
25 is contacted with the second interconnect pattern, whereby the connection step is carried out.

26. The method of manufacture of an interconnect substrate as defined in claim 24,

wherein in the connection step, a part of the first interconnect pattern is bent into the through-holes formed  
5 in the first substrate, and connected to the second interconnect pattern.

27. The method of manufacture of an interconnect substrate as defined in claim 24, wherein:

10 a plurality of through-holes are formed in the second substrate; and

the through-holes formed in the first and second substrates are formed in communicating positions.

15 28. The method of manufacture of an interconnect substrate as defined in claim 27,

wherein in the connection step, a part of the second interconnect pattern is bent into the through-holes formed in the first substrate, and connected to the first  
20 interconnect pattern.

29. The method of manufacture of an interconnect substrate as defined in claim 27,

wherein in the connection step, a part of the first  
25 interconnect pattern and a part of the second interconnect pattern are integrally caused to project from a surface of the second substrate via the through-holes formed in the

second substrate, to form external terminals.

30. The method of manufacture of an interconnect substrate as defined in claim 27,

5        wherein in the connection step, a material for external terminals is contacted with the second interconnect pattern, and provided on the first interconnect pattern via the through-holes formed in the first and second substrates.

10

31. The method of manufacture of an interconnect substrate as defined in any of claims 23 to 30, wherein:

      positioning holes are formed in the first and second substrates; and

15

      before the disposition step, a step is included in which a jig is put into the positioning holes and the first and second substrates are positioned.

20

32. A method of manufacture of an electronic component comprising:

      a disposition step of adhering at least a part of a first substrate on which a first interconnect pattern is formed, having a mounting region for an electronic chip, to a region of a second substrate on which a second  
25 interconnect pattern is formed excluding a mounting region for an electronic chip;

      a connection step of electrically connecting the

first and second interconnect patterns;

a first mounting step of mounting a first electronic chip to be electrically connected to the first interconnect pattern on the first substrate; and

5 a second mounting step of mounting a second electronic chip to be electrically connected to the second interconnect pattern on the mounting region of an electronic chip of the second substrate.

10 33. The method of manufacture of an electronic component as defined in claim 32, wherein:

in the disposition step, a surface of the first substrate opposite to a surface on which the first interconnect pattern is formed is adhered to a surface of  
15 the second substrate on which the second interconnect pattern is formed; and

a plurality of through-holes are formed in the first substrate, and the first interconnect pattern is formed to pass over the through-holes.

20

34. The method of manufacture of an electronic component as defined in claim 33, wherein:

a plurality of through-holes are formed in the second substrate; and

25 the through-holes formed in the first and second substrates are formed in communicating positions.

35. The method of manufacture of an electronic component as defined in claim 34,

wherein in the connection step, a material for external terminals is contacted with the second  
5 interconnect pattern, and provided on the first interconnect pattern via the through-holes formed in the first and second substrates.

36. The method of manufacture of an electronic component  
10 as defined in claim 32,

wherein in the disposition step and the second mounting step, an anisotropic conductive film including conductive particles is provided on a surface of the second substrate on which the second interconnect pattern is  
15 formed, and the first substrate is adhered to the second substrate by means of the anisotropic conductive film, while electrically connecting the second interconnect pattern to the second electronic chip.

20 37. The method of manufacture of an electronic component as defined in claim 32, further comprising:

a step in which the second substrate is bent to adhere the first electronic chip mounted on the first substrate to the second electronic chip mounted on the  
25 second substrate.

38. The method of manufacture of an electronic component

as defined in any of claims 32 to 37,

wherein the disposition step is carried out after the first mounting step.

5 39. The method of manufacture of an electronic component as defined in claim 38, wherein:

the second substrate is a part of a flexible substrate; and

10 the second substrate is formed by stamping out the flexible substrate after the disposition step.

# ABSTRACT

An interconnect substrate comprising: a first substrate (10) on which a first interconnect pattern (12) is formed, having a mounting region (14) for an electronic chip; and a second substrate (20) on which a second interconnect pattern (22) electrically connected to the first interconnect pattern (12) is formed, having a region (26) to which at least a part of the first substrate (10) is adhered, and a mounting region (24) for an electronic chip.

FIG. 1

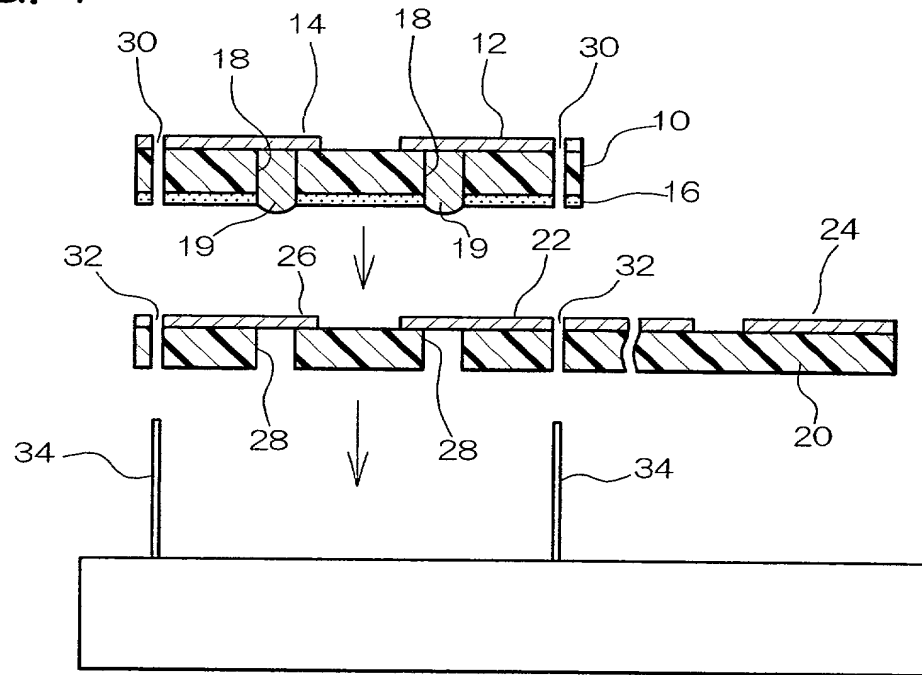
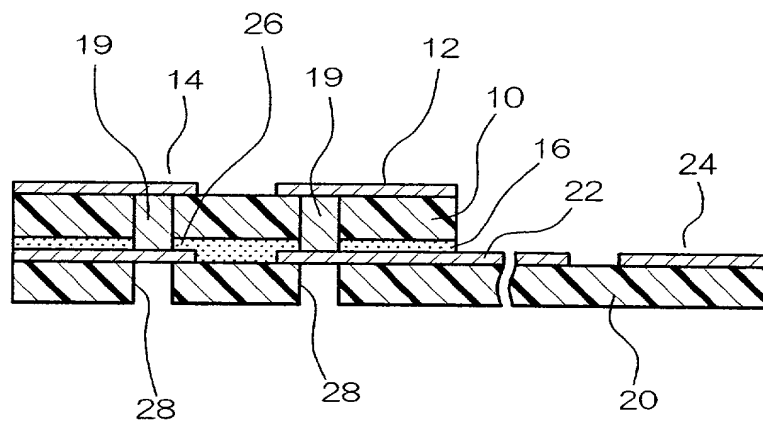


FIG. 2





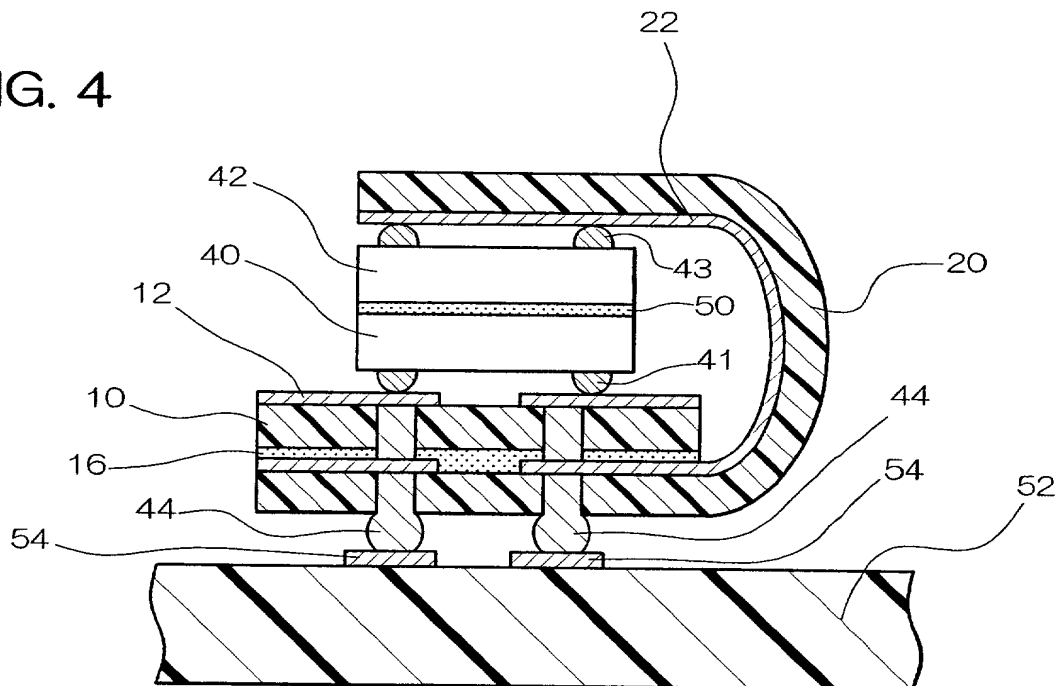


FIG. 5

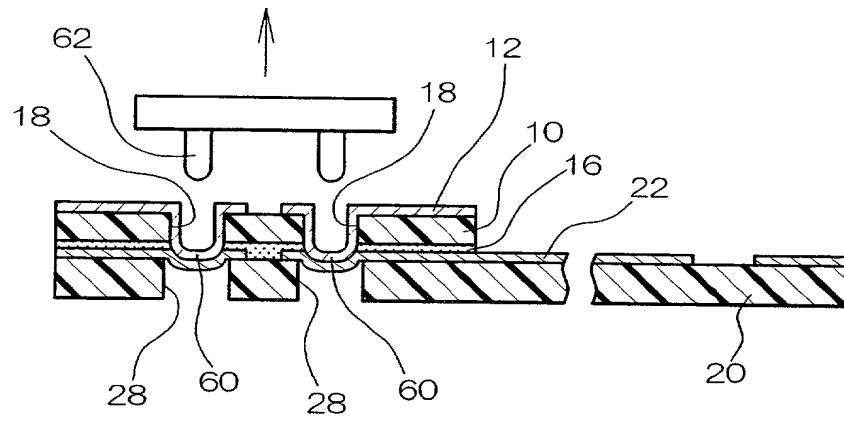


FIG. 6

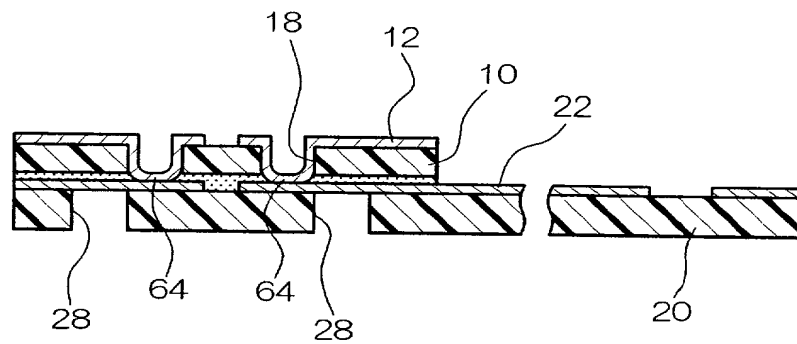


FIG. 7

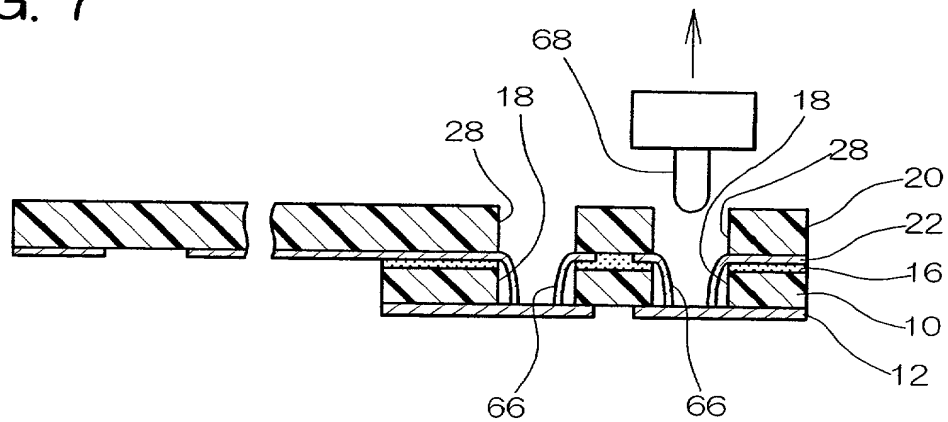


FIG. 8

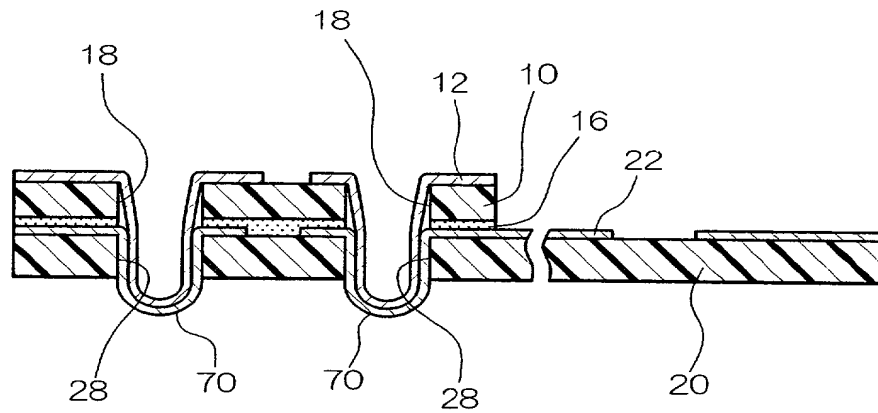


FIG. 9

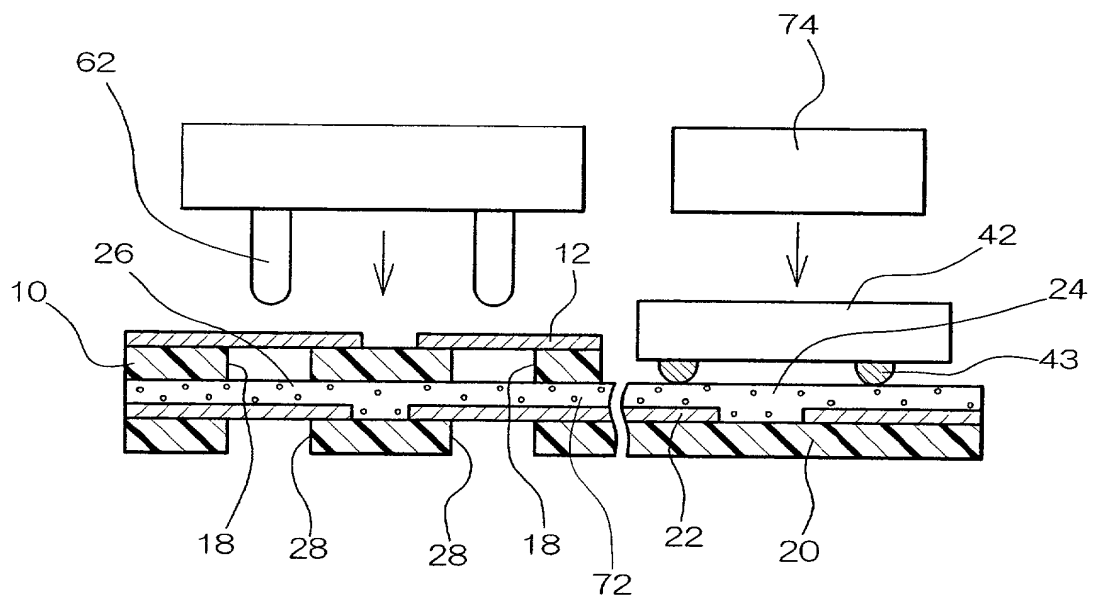


FIG. 10

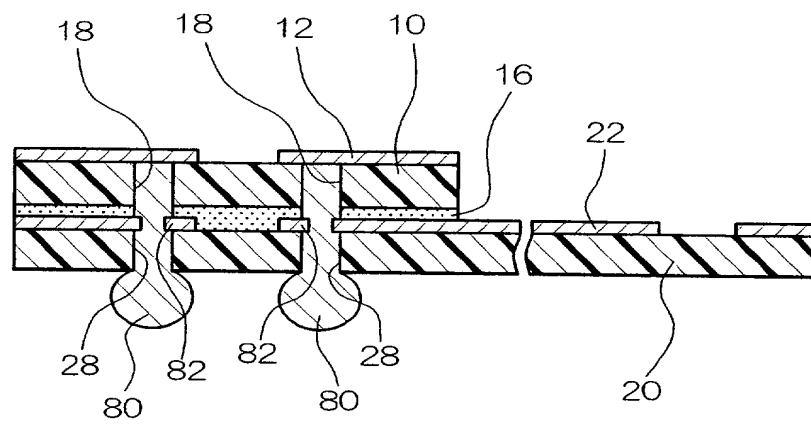
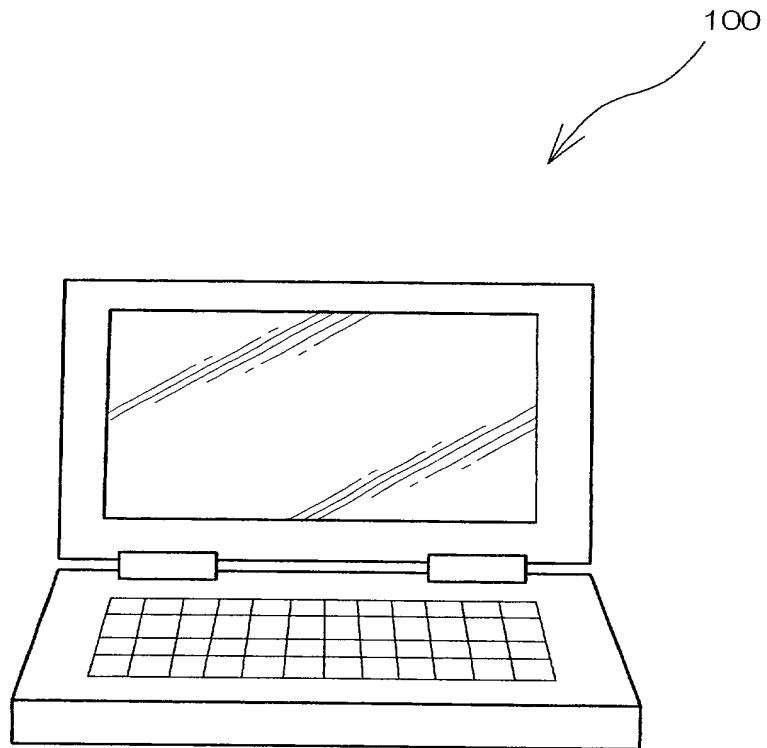


FIG. 11



EPUS-2545

PTO/SB/106 (8-96)

Approved for use through 9/30/98 OMB 0651-0032

Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to collection of information unless it displays a valid OMB control number.

Seiko Epson Ref. No.: F005222US00

Attorney's Ref. No.:

## Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

### Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は、下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

配線基板及びその製造方法、電子部品及びその製造方法、回路基板並びに電子機器

INTERCONNECT SUBSTRATE AND METHOD OF MANUFACTURE THEREOF, ELECTRONIC COMPONENT AND METHOD OF MANUFACTURE THEREOF, CIRCUIT BOARD AND ELECTRONIC INSTRUMENT

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ \_\_\_\_\_に提出され、米国出願番号または  
特許協定条約 国際出願番号を \_\_\_\_\_ とし、  
(該当する場合) \_\_\_\_\_ に訂正されました。

☐ was filed on \_\_\_\_\_  
as United States Application Number or  
PCT International Application Number  
\_\_\_\_\_ and was amended on  
\_\_\_\_\_ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

## Japanese Language Declaration

(日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基づき下記の、米国以外の国の少なくとも1ヶ国を指定している特許協力条約365条(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

## Prior Foreign Application(s)

外国での先行出願

Priority Not Claimed

優先権主張なし

<u>11-232565(P)</u>	<u>Japan</u>	<u>19/August/1999</u>
(Number)	(Country)	(Day/Month/Year Filed)
(番号)	(国名)	(出願年月日)
 <u>                    </u>	 <u>                    </u>	 <u>                    </u>
(Number)	(Country)	(Day/Month/Year Filed)
(番号)	(国名)	(出願年月日)

☐☐

私は、第35編米国法典119条(e)項に基づいて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119 (e) of any United States provisional application(s) listed below.

<u>                    </u>	<u>                    </u>	<u>                    </u>	<u>                    </u>
(Application No.)	(Filing Date)	(Application No.)	(Filing Date)
(出願番号)	(出願日)	(出願番号)	(出願日)

私は下記の米国法典第35編120条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365 (c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application:

<u>PCT/JP00/05395</u>	<u>11/August/2000</u>	<u>Pending</u>
(Application No.)	(Filing Date)	(Status: Patented, Pending, Abandoned)
(出願番号)	(出願日)	(現況: 特許許可済、係属中、放棄済)
 <u>                    </u>	 <u>                    </u>	 <u>                    </u>
(Application No.)	(Filing Date)	(Status: Patented, Pending, Abandoned)
(出願番号)	(出願日)	(現況: 特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私が入手した情報と私の信じることに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

## Japanese Language Declaration

(日本語宣言書)

委任状： 私は、下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁護士、または代理人の氏名及び登録番号を明記のこと)

James A. Oliff, (Reg. 27,075)  
 William P. Berridge, (Reg. 30,024)  
 Kirk M. Hudson, (Reg. 27,562)  
 Thomas J. Pardini, (Reg. 30,411)  
 Edward P. Walker, (Reg. 31,450)  
 Robert A. Miller, (Reg. 32,771)  
 Mario A. Costantino, (Reg. 33,565)  
 Caroline D. Dennison, (Reg. 34,494)

16

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

James A. Oliff, (Reg. 27,075)  
 William P. Berridge, (Reg. 30,024)  
 Kirk M. Hudson, (Reg. 27,562)  
 Thomas J. Pardini, (Reg. 30,411)  
 Edward P. Walker, (Reg. 31,450)  
 Robert A. Miller, (Reg. 32,771)  
 Mario A. Costantino, (Reg. 33,565)  
 Caroline D. Dennison, (Reg. 34,494)

書類送付先:

OLIFF & BERRIDGE, PLC  
 P.O. Box 19928  
 Alexandria, Virginia 22320

Send Correspondence to:

OLIFF & BERRIDGE, PLC  
 P.O. Box 19928  
 Alexandria, Virginia 22320

直接電話連絡先: (名前及び電話番号)

OLIFF & BERRIDGE, PLC  
 (703) 836-6400

Direct Telephone Calls to: (name and telephone number)

OLIFF & BERRIDGE, PLC  
 (703) 836-6400

唯一または第一発明者名

橋元 伸晃

Full name of sole or first inventor

Nobuaki HASHIMOTO

発明者の署名

日付

橋元 伸晃

2001年 4月 6日

Inventor's signature

Date

Nobuaki Hashimoto

April 6, 2001

住所

日本国

長野県

諏訪市

Residence

Suwa-shi, Nagano-ken, Japan

国籍

日本

Citizenship

Japan

JPL

私書箱

392-8502 日本国長野県諏訪市大和3丁目3番5号  
 セイコーエプソン株式会社内

Post Office Address

c/o Seiko Epson Corporation

3-5, Owa 3-chome, Suwa-shi, Nagano-ken 392-8502 Japan

第二共同発明者

Full name of second joint inventor, if any

第二共同発明者の署名

日付

Second inventor's signature

Date

住所

日本国

Residence

Japan

国籍

Citizenship

私書箱

Post Office Address

(第三以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for third and subsequent joint inventors.)